

## CLAIMS

What is claimed is:

- 1 1. A method, comprising:
  - 2 a) measuring a skew between a data signal and a clock signal at a
  - 3 receiving end of a serial link; and
  - 4 b) adjusting a phase relationship between said data signal and said
  - 5 clock signal to reduce said skew.
- 6 2. The method of claim 1 wherein said adjusting of said phase relationship
- 7 occurs at a transmitting end of said serial link.
- 1 3. The method of claim 1 further comprising receiving said measured skew at
- 2 a skew adjustment unit and determining said phase relationship before said
- 3 adjusting a phase relationship.
- 1 4. The method of claim 1 further comprising programming said phase
- 2 relationship into a semiconductor chip.
- 1 5. The method of claim 1 wherein said adjusting a phase relationship further
- 2 comprises imposing a delay on at least one of said signals.
- 1 6. The method of claim 5 wherein said adjusting a phase relationship further
- 2 comprises imposing a delay on both of said signals.
- 1 7. The method of claim 1 wherein said adjusting a phase relationship further
- 2 comprises adjusting a phase offset between a pair of phasors associated with a
- 3 pair of phase interpolators, a first of said phasors used to derive a second clock

4 signal that times the transmission of said data signal, a second of said phasors  
5 used to derive said clock signal.

1 8. An apparatus, comprising:

2 a) a transmitting unit coupled to a receiving unit by a serial link, said  
3 serial link configured to transport a clock signal and a data signal;

4 b) a skew measurement unit coupled to said serial link such that said  
5 coupling of said skew measurement unit to said serial link is closer to said  
6 receiving unit than said transmitting unit; and

7 c) a skew adjustment unit coupled to said skew adjustment and said  
8 transmitting unit.

1 9. The apparatus of claim 8 further comprising a programmable delay unit  
2 within said transmitting unit, said programmable delay unit coupled to said skew  
3 adjustment unit, said programmable delay unit output corresponding to one of  
4 said signals.

1 10. The apparatus of claim 8 further comprising a second programmable delay  
2 unit within said transmitting unit, said second programmable delay unit coupled  
3 to said skew adjustment unit, said programmable delay unit output  
4 corresponding to another of said signals.

1 11. The apparatus of claim 9 wherein said programmable delay unit further  
2 comprises a cascade of inverters.

1 12. The apparatus of claim 11 wherein each of said inverters within said  
2 cascade of inverters has an adjustable propagation delay.

1 13. The apparatus of claim 8 wherein transmission of said data signal is timed  
2 according to a phase interpolator output.

1 14. The apparatus of claim 8 wherein clock signal is derived from a phase  
2 interpolator output.

1 15. The apparatus of claim 14 wherein said phase interpolator further  
2 comprises a skew control input that adjusts a phasor phase offset, said skew  
3 control input coupled to said skew adjustment unit.

1 16. The apparatus of claim 8 wherein said skew adjustment unit further  
2 comprises a CPU.

1 17. An apparatus, comprising:

- 2 a) a network interface coupled to a transmitting unit;  
3 b) a receiving unit coupled to said transmitting unit by a serial link,  
4 said serial link configured to transport a clock signal and a data signal;  
5 c) a skew measurement unit coupled to said serial link such that said  
6 coupling of said skew measurement unit to said serial link is closer to said  
7 receiving unit than said transmitting unit; and  
8 d) a skew adjustment unit coupled to said skew adjustment and said  
9 transmitting unit.

1 18. The apparatus of claim 17 wherein transmission of said data signal is timed  
2 according to a phase interpolator output.

1 19. The apparatus of claim 17 wherein clock signal is derived from a phase  
2 interpolator output.

1 20. The apparatus of claim 19 wherein said phase interpolator further  
2 comprises a skew control input that adjusts a phasor phase offset, said skew  
3 control input coupled to said skew adjustment unit.

1 21. The apparatus of claim 17 wherein said skew adjustment unit further  
2 comprises a CPU.

1 22. The apparatus of claim 17 wherein said transmitting unit further comprises  
2 a parallel to serial converter that crafts said data signal, said parallel to serial  
3 converter receiving parallel data from said network interface.

1 23. The apparatus of claim 17 wherein said network interface corresponds to a  
2 physical layer.

1 24. The apparatus of claim 17 wherein said network interface corresponds to a  
2 media access control layer.